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Serial No.:
Inventor(s): Doan et al.

What is Claimed is:

1. A method for fabricating a semiconductor wafer, comprising the steps of:

5 a) forming a first layer superjacent a semiconductor substrate;

b) Forming a film superjacent said first layer, said film having a structural integrity;

c) forming a second layer superjacent said film; and

10 d) heating said substrate sufficiently to cause said first layer and said second layer to uniformly reflow.

2. A method for fabricating a semiconductor wafer, according to Claim 1, wherein said heating comprises the step of:

expanding said first layer according to a first thermal coefficient;

15 expanding said second layer according to a second thermal coefficient; and

Serial No.:
Inventor(s): Doan et al.

maintaining said structural integrity of said film,
thereby enabling said first and said second layers to reflow
uniformly.

3. A method for fabricating a semiconductor wafer, according
5 to Claim 2, wherein said film isolates said first layer from
said second layer, thereby preventing said first layer and
said second layer from interacting during said heating step.

4. A method for fabricating a semiconductor wafer, according
to Claim 2, wherein said heating step is at least at a
10 temperature of approximately 700°C.

5. A method for fabricating a semiconductor wafer, according
to Claim 2, wherein said forming a film comprises the step of:

exposing said substrate to a gas and radiant energy.

6. A method for fabricating a semiconductor wafer, according
15 to Claim 5, wherein said gas comprises at least one of N₂, NH₃,
O₂, N₂O, Ar, Ar-H₂, H₂, GeH₄, and a Fluorine based gas.

Serial No.:
Inventor(s): Doan et al.

7. A method for fabricating a semiconductor wafer, according to Claim 6, wherein said radiant energy generates heat substantially within the range of 500°C to 1250°C and said substrate is exposed to said gas for approximately 5 seconds
5 to 60 seconds at a flow rate substantially in the range of 50 sccm to 20,000 sccm.

8. A method for fabricating a semiconductor wafer, according to Claim 5, wherein said film comprises at least one of titanium nitride, tantalum nitride, titanium oxide, tantalum
10 oxide, silicon dioxide, silicon nitride and tetraethylorthosilicate ("TEOS").

9. A method for fabricating a semiconductor wafer, according to Claim 8, wherein said first layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal
15 silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

Serial No.:
Inventor(s): Doan et al.

10. A method for fabricating a semiconductor wafer, according to Claim 8, wherein said second layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon,
5 borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

11. A method for reducing the effects of buckling in fabricating a semiconductor wafer, comprising the steps of:

a) forming a planarization layer superjacent a
10 semiconductor substrate;

b) forming a barrier film superjacent said planarization layer, said barrier film having a structural integrity;

c) forming a second layer superjacent said barrier
15 film; and

d) heating said substrate sufficiently to cause said planarization layer to expand according to a first thermal coefficient of expansion, said second layer to expand

Serial No.:
Inventor(s): Doan et al.

according to a second thermal coefficient of expansion, while said structural integrity of said barrier film is maintained, thereby enabling said planarization layer and said second layer to uniformly reflow.

5 12. A method for fabricating a semiconductor wafer, according to Claim 11, wherein said barrier film isolates said planarization layer from said second layer, thereby preventing said planarization layer and said second layer from interacting during said heating step.

10 13. A method for fabricating a semiconductor wafer, according to Claim 11, wherein said heating step is at least at a temperature of approximately 700°C.

15 14. A method for fabricating a semiconductor wafer, according to Claim 11, wherein said forming a barrier film comprises the step of:

exposing said substrate to a gas and radiant energy, said gas comprising at least one of N₂, NH₃, O₂, N₂O, Ar, Ar-H₂, H₂,

Serial No.:
Inventor(s): Doan et al.

GeH_4 , and a Fluorine based gas, said radiant energy generating heat substantially within the range of 500°C to 1250°C.

15. A method for fabricating a semiconductor wafer, according to Claim 11, wherein said barrier film comprises at least one
5 of titanium nitride, tantalum nitride, titanium oxide, tantalum oxide, silicon dioxide, silicon nitride and tetraethylorthosilicate ("TEOS").

16. A method for fabricating a semiconductor wafer, according to Claim 15, wherein said planarization layer comprises at
10 least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

17. A method for fabricating a semiconductor wafer, according to Claim 16, wherein said second layer comprises at least one
15 of tungsten, titanium, tantalum, copper, aluminum, single

Serial No.:
Inventor(s): Doan et al.

crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

18. A method for fabricating semiconductor wafers
5 substantially impervious to the effects of buckling,
comprising the steps of:

a) forming a planarization layer superjacent a
semiconductor substrate, said planarization layer comprising
at least one of tungsten, titanium, tantalum, copper,
10 aluminum, single crystal silicon, polycrystalline silicon,
amorphous silicon, borophosphosilicate glass ("BPSG") and
tetraethylorthosilicate ("TEOS");

b) forming a barrier film having a structural integrity
superjacent said planarization layer by exposing said
15 substrate to a gas and radiant energy, said gas comprising at
least one of N₂, NH₃, O₂, N₂O, Ar, Ar-H₂, H₂, GeH₄, and a
Fluorine based gas, said radiant energy generating heat
substantially within the range of 500°C to 1250°C;

Serial No.:

Inventor(s): Doan et al.

c) forming another layer superjacent said barrier film, said another layer comprising at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS");

d) heating said substrate sufficiently to at least at a temperature of approximately 700°C to cause said planarization layer to expand according to a first thermal coefficient of expansion, said another layer to expand according to a second thermal coefficient of expansion, and said structural integrity of said barrier film to be maintained, said barrier film isolating said planarization layer from said another layer, thereby preventing said planarization layer and said another layer from interacting during said heating, and enabling said planarization layer and said another layer to reflow uniformly.

Serial No.:
Inventor(s): Doan et al.

19. A semiconductor device substantially impervious to the effects of buckling, said device comprising:

a) a first layer superjacent a semiconductor substrate;

b) a barrier film superjacent said substrate, said
5 barrier film having a structural integrity; and

c) a second layer superjacent said barrier film, said
second layer being isolated from said first layer by said
barrier film when a temperature of at least approximately
700°C is applied, thereby preventing said first layer and
10 said second layer from interacting, and enabling said
first layer and said second layer to uniformly reflow.

20. A semiconductor device substantially impervious to the effects of buckling, according to Claim 19, wherein said barrier film comprises at least one of titanium nitride, tantalum nitride, titanium oxide, tantalum oxide, silicon
15 dioxide, silicon nitride and tetraethylorthosilicate ("TEOS").

Serial No.:
Inventor(s): Doan et al.

21. A semiconductor device substantially impervious to the effects of buckling, according to Claim 19, wherein said first layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

22. A semiconductor device substantially impervious to the effects of buckling, according to Claim 19, wherein said second layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").